



SANYO Semiconductors

DATA SHEET

LA6220M

Monolithic Linear IC
 Rail-to-Rail
 Dual Operational Amplifier

Overview

The LA6220M dual operational amplifier is optimal for both consumer and industrial applications, including all types of transducer amplifier and DC amplifier circuit. It supports from ground to V_{CC} (rail to rail) as the voltage range for both inputs and outputs. It is optimal for the amplification of signals from all types of sensors.

Functions

- Does not require phase compensation
- Supports from ground to V_{CC} (rail to rail) as the voltage range for both inputs and outputs
- Low current dissipation : $I_{CC} = 1.2\text{mA typ}/V_{CC} = +5\text{V}$, $R_L = \infty$

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		18	V
Differential input voltage	V_{ID}		± 1	V
Maximum input voltage	$V_{IN\text{ max}}$		-0.3 to +18	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 25^\circ\text{C}$ Mounted on specified board. *	0.8	W
Operating temperature	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Specified board size : $114.3 \times 76.1 \times 1.6\text{mm}^3$, glass epoxy.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2 to 17	V

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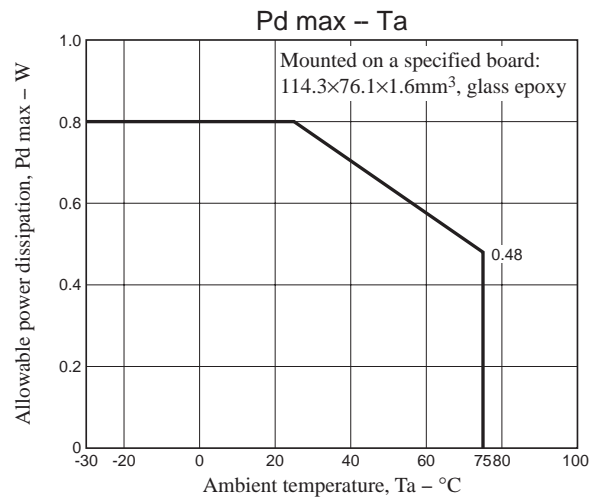
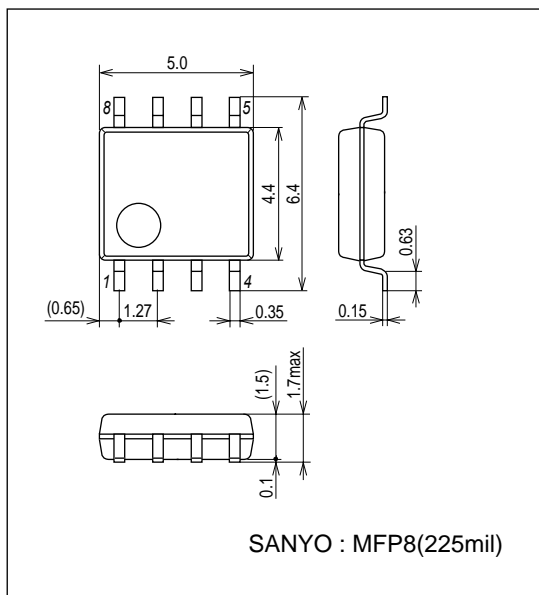
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, Otherwise unless specified.

Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Input offset voltage	V_{IO}		1		± 2	± 7	mV
Input offset current	I_{IO}	$I_{IN (+)}/I_{IN (-)}$	2		± 5	± 50	nA
Input bias current	I_B	$I_{IN (+)}/I_{IN (-)}$	3, 4		45	250	nA
Common-mode input voltage range	V_{ICM}		5	0		V_{CC}	V
Common-mode rejection ration	CMR		5		80		dB
Large amplitude voltage	VG		6		100		V/mV
Output voltage range	V_{OH1A}	$R_L = 20\text{k}\Omega$: $T_a = 25^\circ\text{C}$	12	4.9			V
	V_{OH1B}	$R_L = 20\text{k}\Omega$: $T_a = -40$ to 85°C	12	4.85			V
	V_{OL1}	$R_L = 20\text{k}\Omega$	12			0.1	V
Output voltage range	V_{OH2}	$R_L = 2\text{k}\Omega$	12	4.75			V
	V_{OL2}	$R_L = 2\text{k}\Omega$	12			0.25	V
Supply voltage rejection ratio	SVR		11		80		dB
Channel separation	CS	$f = 1\text{kHz}$ to 20kHz	7		80		dB
Current drain	I_{CC}		8		1.2	2.5	mA
Output current (source)	$I_{O \text{ source}}$	$V_{IN+} = 1\text{V}$, $V_{IN-} = 0\text{V}$	9	6	10		mA
Output current (sink)	$I_{O \text{ sink}}$	$V_{IN+} = 0\text{V}$, $V_{IN-} = 1\text{V}$	10	3	5		mA
Slew rate	SR	$R_L = 2\text{k}\Omega$			0.35		V/ μs
Gain-bandwidth product	F_t	$R_L = 2\text{k}\Omega$			1		MHz
Phase margin	ϕ_M	$R_L = 2\text{k}\Omega$			80		Deg

Package Dimensions

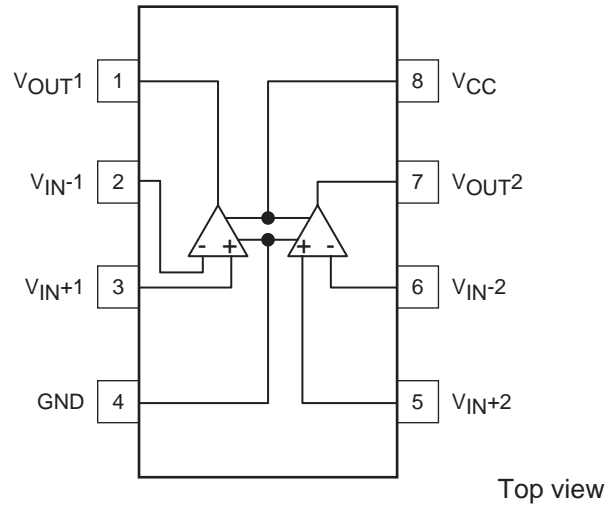
unit : mm (typ)

3032D



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Pin Assignment

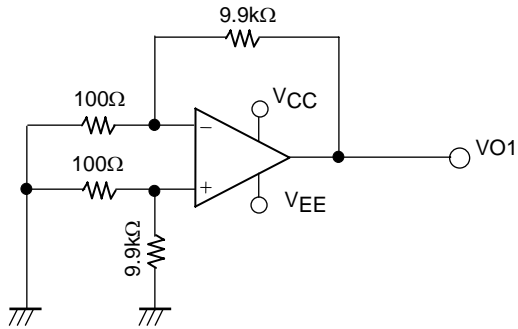


Pin Description

Pin No.	Symbol	function	Equivalent circuit
3 2 5 6	V_{IN+1} V_{IN-1} V_{IN+2} V_{IN-2}	Noninverting inputs 1 Inverting inputs 1 Noninverting inputs 2 Inverting inputs 2	
1 7	V_{OUT1} V_{OUT2}	Outputs 1 Outputs 2	

Test Circuits

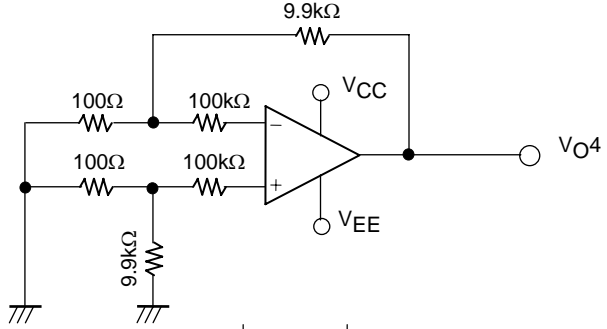
1. Input offset voltage V_{IO}



$$V_{CC}/V_{EE} = \pm 2.5V$$

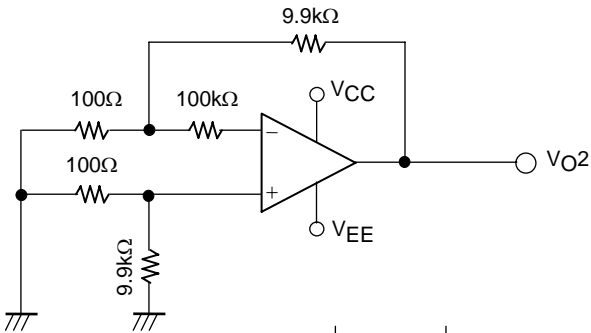
$$V_{IO} = V_{O1}/100$$

2. Input offset current I_{IO}



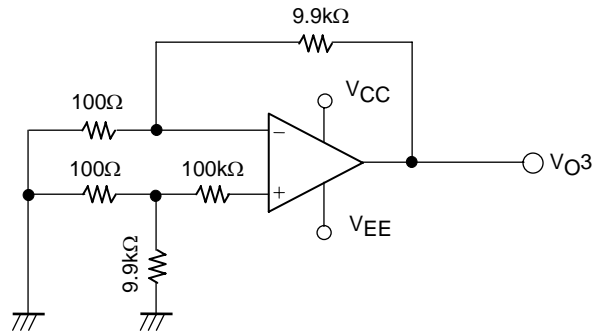
$$I_{IO} = \frac{|V_{O4} - V_{O1}|}{100k\Omega \times 100}$$

3. Input bias current $I_B (-)$



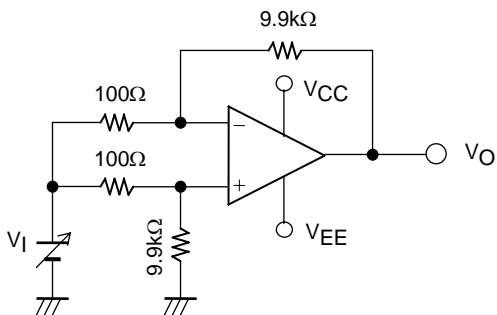
$$I_{B(-)} = \frac{|V_{O2} - V_{O1}|}{100k\Omega \times 100}$$

4. Input bias current $I_B (+)$



$$I_{B(+)} = \frac{|V_{O3} - V_{O1}|}{100k\Omega \times 100}$$

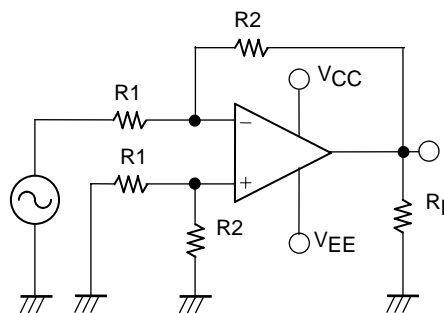
5. Common-mode rejection ratio (CMR)
Common-mode input voltage range (VICM)



$$CMR \ V_1 = \pm 2.5V$$

$$CMR = 20\log (5 \times 100 / |\Delta V_{O1}|)$$

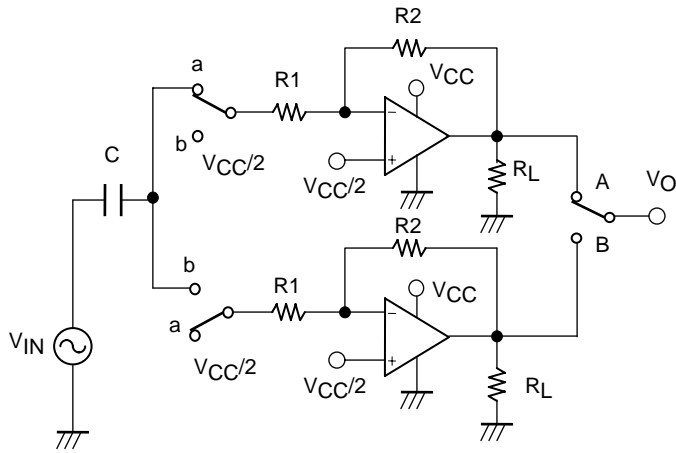
6. Voltage gain (VG)



$$VG = \frac{R2}{R1}$$

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7. Channel separation (CS)



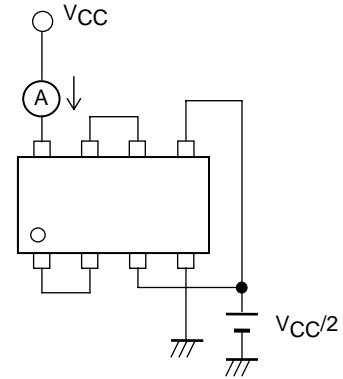
When the switch is the "a" position.

$$CS(A \rightarrow B) = 20 \log \frac{R2V_{OA}}{R1V_{OB}}$$

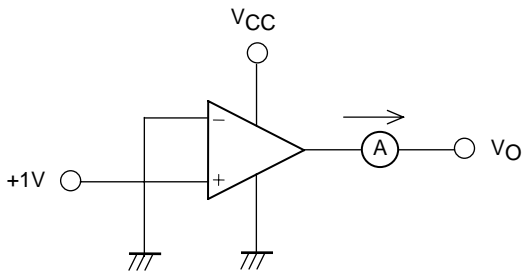
When the switch is the "b" position.

$$CS(B \rightarrow A) = 20 \log \frac{R2V_{OB}}{R1V_{OA}}$$

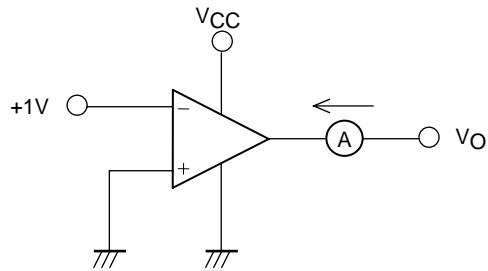
8. Current drain (ICC)



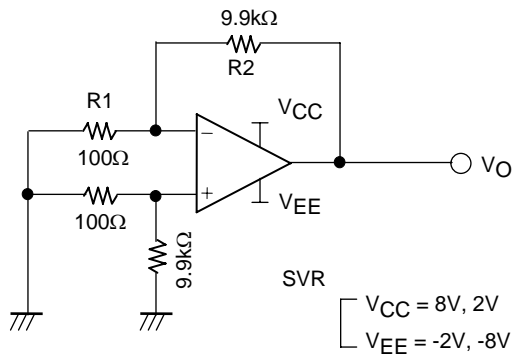
9. Output current (I_{Osource})



10. Output current (I_Osink)



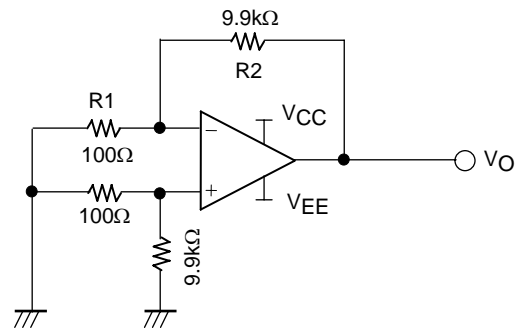
11. Supply voltage rejection ratio SVR (+)



SVR
 $V_{CC} = 8V, 2V$
 $V_{EE} = -2V, -8V$

$$SVR(+)=20 \log \left| \frac{\Delta V_{CC} \times 100}{\Delta V_O} \right|$$

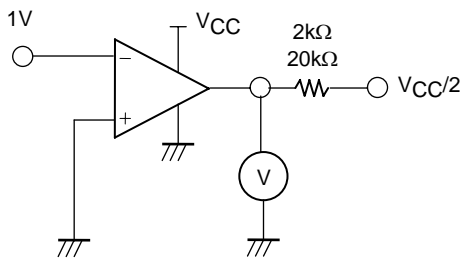
12. Supply voltage rejection ratio SVR (-)



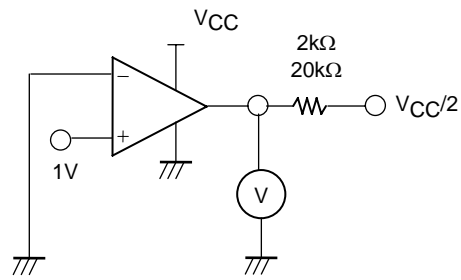
$$SVR(-)=20 \log \left| \frac{\Delta V_{EE} \times 100}{\Delta V_O} \right|$$

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13. Output voltage range (Isink)



14. Output voltage range (Isource)



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